REMARKS

Claims 1-12 are pending in the application. It is gratefully acknowledged that Claims 6 and 8 remain objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims. Claims 1-12 were rejected under 35 U.S.C. §112, first and second paragraphs. Claims 1-5, 7 and 9-12 were rejected under 35 U.S.C. §102(e) as being anticipated by Suda et al. (U.S. Patent 6,553,516).

Please cancel Claims 2 and 6 without prejudice. Please amend Claims 1 and 10 as set forth herein. No new matter has been added.

Regarding the §112, first and second paragraph, rejections, the Examiner contends that "wherein the address calculator calculates the finally interleaved address without ... generating an intra-row permutation basic sequence" of Claim 1, and "wherein the read address is determined without...generating an intra-row permutation basic sequence" of Claim 10, are not enabled by the specification and are indefinite. Claims 1 and 10 have been amended to delete this language. Based on at least the foregoing, withdrawal of the rejections of independent Claims 1 and 10 under §102(e) is respectfully requested.

Regarding the rejections of independent Claims 1 and 10 under §102(e), the Examiner states that Suda et al. anticipates the claims. Suda et al. discloses an interleaving method, interleaving apparatus, turbo encoding method, and turbo encoder. Claim 1 has been amended to incorporate the allowable subject matter of Claims 2 and 6, and Claim 10 has been amended to include the allowable subject matter of Claim 6, in method form.

Based on at least the foregoing, withdrawal of the rejections of independent Claims 1 and 10 under §102(e) is respectfully requested.

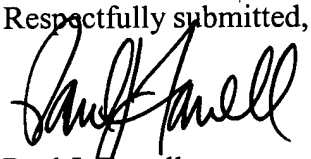
As further guidance for proper examination of this application, the following is provided.

Regarding the rejection under §102(e), FIG. 5 of Suda et al., illustrates the steps of storing a result of the inter-permutation in a memory; and storing the rearranged data obtained by the intra-permutation, after performing the intra-permutation. In other words, Suda et al. must store the inter-permutation pattern based on a permutation pattern, which varies according to the number of the input bits, and must include a memory for storing a result of the inter-permutation based on the permutation pattern. Thus, Suda et al. has a problem in that the intra/inter-permutation pattern corresponding to the number of the input bits must be stored, which was pointed out as a problem of conventional art in the Background section of the present application. On the contrary, the claims of the present application claim an advantage in calculating an intra-permutation pattern by using an increment incr(j) and storing the calculated data, thereby decreasing the use of a memory. Suda et al. does not suggest or teach using an increment, and Suda et al. has a problem in that all of the permutation patterns must be stored in the memory.

Independent Claims 1 and 10 are believed to be in condition for allowance. Without conceding the patentability per se of dependent Claims 3-5, 7, 9, 11 and 12, these are likewise believed to be allowable by virtue of their dependence on their respective amended independent claims. Accordingly, reconsideration and withdrawal of the rejections of dependent Claims 3-5, 7, 9, 11 and 12 is respectfully requested.

Accordingly, all of the claims pending in the Application, namely, Claims 1, 3-5 and 7-12, are believed to be in condition for allowance. Should the Examiner believe that a telephone conference or personal interview would facilitate resolution of any remaining matters, the Examiner may contact Applicant's attorney at the number given below.

Respectfully submitted,



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